REMARKS

Claims 2-7, 9, 11, 14-16, 39, and 45-49 were presented for examination. Claims 2-7, 9, 11, 14-16, 39, and 45-49 were rejected. Independent claims 7, 9, 11, 14, 16 and 39 have been amended.

Rejections Under 35 U.S.C. § 102(b)

In the most recent Office Action, claims 5-7, 11, 14-16 and 46, 47, and 49 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tsutsumi. Applicant respectfully traverses this rejection.

Claim 7, as amended, recites, in part, a method for fabricating a semiconductor device. A dielectric layer is formed over the base substrate. A damascene trench is formed in the first dielectric layer. The damascene trench has both a gate area and a local interconnect area. A gate oxide layer is formed on the base substrate within the gate area. Conductive material is deposited over the base substrate to fill the damascene trench. The device is then planed to define a damascene structure where the damascene gate structure and damascene local interconnect structure are formed in a single mask and etch process and are electrically coupled by the conductive material within the damascene trench. In addition, a connection between the damascene local interconnect structure and the base substrate is formed.

Tsutsumi discloses a method for simultaneously fabricating a gate electrode opening and interconnection groove in a semiconductor device. However, Tsutsumi fails to disclose a connection between the interconnection groove 31 and the semiconductor substrate 1 when the gate electrode opening 8 and interconnection groove 31 are formed during a single process. Tsutsumi, instead, discloses forming the interconnect 32 on top of the second insulting film 3 which is not in connection with the semiconductor substrate 1, or base substrate (Figs. 60, 66, 68,

73 and 75). This limitation is not found in the claimed invention. Because Tsutsumi does not disclose a connection between the damascene local interconnection and the semiconductor substrate when the gate electrode opening and interconnection groove are formed during a single process, Tsutsumi does not recite all the limitations of the claimed invention. Therefore, Applicant asserts that claim 7 is not anticipated by Tsutsumi and requests that the Examiner withdraw his rejection of claim 7.

Independent claims 11, 14 and 16 also recite the limitation of a connection between the damascene local interconnect structure and the base substrate when the gate and local interconnect are formed during a single process as recited in claim 7. Therefore, for the same reasons stated above, Applicant asserts that these claims are also not anticipated by Tsutsumi and requests that the Examiner withdraw his rejection of claims 11, 14 and 16.

Claims 5, 6, 15, 46, 47, and 49 depend on independent claims 7, 11, 14, and 16 either directly or ultimately. These dependent claims are patentable for the same reasons as presented above with respect to the claims from which they depend. Therefore, Applicant asserts that claims 5, 6, 15, 46, 47, and 49 are also not anticipated by Tsutsumi and requests that the Examiner withdraw his rejection thereof.

Rejections Under 35 U.S.C. § 103(a)

Claims 2, 3, 39, 45, and 48 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsutsumi in view of the basic text of Ghandi. Applicant respectfully traverses this rejection.

Claim 39, as amended, recites, in part, growing an oxide layer on the base substrate. A second patterned mask is formed over the semiconductor device and is arranged to expose at least a portion of the oxide layer within the area that will be the local interconnect. The exposed portion of said oxide layer is then etched away within said damascene trench.

In contrast, because Tsutsumi fails to disclose a connection between the interconnection groove and the semiconductor substrate, it is not possible to grow an oxide layer on the

sem conductor substrate exposed in the interconnection groove since no semiconductor substrate is exposed in the interconnection groove. Instead, Tsutsumi discloses forming the interconnection 32 on top of the second insulting film 3 and not on the semiconductor substrate 1 (Figs. 60, 66, 68, 73 and 75) as discussed more fully above.

Examiner admits Tsutsumi fails to teach a trench formed in the base substrate and cites Ghandi. However, Ghandi fails to remedy the deficiencies of Tsutsumi. Ghandi discloses using thermal oxidation to reduce leakage current. However, Ghandi fails to disclose growing an oxide layer on the base substrate exposed in the interconnection groove. Therefore, neither Tsutsumi nor Ghandi disclose this limitation of the claimed invention.

Nor does the hypothetical combination of Tsutsumi and Ghandi suggest or teach growing an oxide layer on the base substrate exposed in the interconnection groove. At best, the hypothetical combination of Tsutsumi and Ghandi teaches forming the interconnection on top of a insulting film and using thermal oxidation to form the isolation trench. Because the hypothetical combination of Tsutsumi and Ghandi does not suggest or teach all the limitations of the claimed invention, Applicant asserts that claim 39 is patentable over the prior art and requests that the Examiner withdraw his rejection of claim 39.

Claims 2, 3, 45 and 48 depend upon the independent claims 7 and 39 either directly or ultimately. These dependent claims are patentable for the same reasons as presented above with respect to the claims from which they depend. Therefore, Applicant believes claims 2, 3, 45 and 48 are also patentable over the prior art and request the Examiner withdraw his rejection to claims 2, 3, 45 and 48.

Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsutsumi in view of Zhou. Applicant respectfully traverses this rejection.

Claim 4 depends on independent claim 7. Applicant believes Claim 7 as amended is patentable over the prior art for the reasons stated above. Claim 4 is patentable for the same reasons as presented above with respect to claims 7 from which it depends. Therefore, Applicant

asserts that claim 4 is also patentable over the prior art and requests that the Examiner withdraw his rejection of claim 4.

Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsutsumi. Applicant respectfully traverses this rejection.

Claim 9, as amended, also recites a connection between the damascene local interconnect structure and the base substrate when the gate and local interconnect are formed during a single process as discussed above for claim 7.

As mentioned above, Tsutsumi fails to disclose a connection between the interconnection and the semiconductor substrate. Instead, Tsutsumi discloses forming the interconnection 32 on top of the second insulting film 3 and not on the semiconductor substrate 1 (Figs. 60, 66, 68, 73 and 75). Therefore, for the same reasons mentioned above, Applicant asserts that claim 9 is not anticipated by Tsutsumi and requests that the Examiner withdraw his rejection of claim 9.

Official Amendment
Serial No. 09/943,078
Docket : MIO 0083 PA/40509.162

CONCLUSION

For the above reasons, the Applicant respectfully submits that the above claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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